Short Course On

Modeling and Simulation of Nano-Transistors

February 13 - 17, 2017

Organized by Department of Electrical Engineering, IIT Kanpur

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Website

http://www.iitk.ac.in/nanolab/sc2017

Registration Form

http://www.iitk.ac.in/nanolab/sc2017

Registration Fee **

Faculty: Rs. 10,000
Industry/R&D Labs: Rs. 20,000
Students: Rs. 5,000

Coordinators

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Contact

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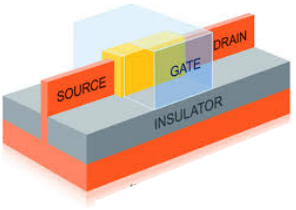
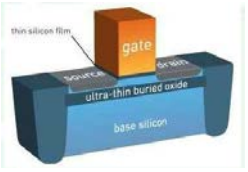
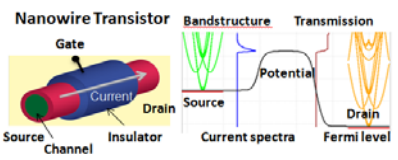
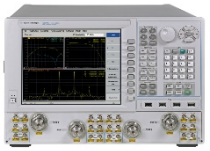
Topics:



- VLSI design and Nanoelectronics
- Physics and Operation of MOSFET
- SPICE and Circuit simulation
- TCAD simulation: Theory and demonstration
- Compact Modeling: Theory and demonstration
- Scaling and Moore's Law
- International Technology Roadmap for Semiconductors
- Nano-Transistors: FinFET, FDSOI, Negative Capacitance FET
- Characterization: Current and capacitance measurement
- RF CMOS and GaN High Electron Mobility Transistors







Also included:

- Laboratory visits and RF transistor measurement
- New research problems in Nanoelectronics
- How to write research project and papers

Target Audience:

Faculty members, practicing engineers & students.

SPEAKERS

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****Registration Fee includes course fee, accommodation, food, printed lecture notes and stationery.**